CLAIMS

What is claimed is:

1. An image signal processor comprising:

a local memory to store data; and

a memory command handler including a plurality of memory address generators, each memory address generator to generate a memory address to the local memory and to interpret a command to be performed on the data of the local memory located at the memory address to aid in image processing tasks.

2. The image signal processor of claim 1, further comprising a shared memory coupled to the plurality of the memory address generators, the shared memory storing data to be sent to the local memory and commands to be performed by the memory address generators.

3. The image signal processor of claim 2, wherein the shared memory comprises a plurality of cluster communication registers.

4. The image signal processor of claim 3, further comprising a cluster communication register interface to couple the plurality of cluster communication registers to the plurality of memory address generators.

5. The image signal processor of claim 3, wherein the plurality of cluster communication registers include data cluster communication registers to store data and command cluster communication registers to store commands.

6. The image signal processor of claim 5, wherein a pair of cluster communication registers are assigned to each memory address generator.

7. The image signal processor of claim 6, wherein each pair of cluster communication registers includes a data cluster communication register and a command cluster communication register.

8. The image signal processor of claim 3, further comprising an arbiter to arbitrate access to the local memory by the memory address generators.

9. The image signal processor of claim 8, wherein the plurality of cluster communication registers are at least 16-bit registers.

10. The image signal processor of claim 9, further comprising 16-bit data paths that couple the cluster communication registers to the memory address generators, the memory address generators to the arbiter, and the arbiter to the local memory.

11. The image signal processor of claim 10, wherein the local memory includes static random access memory (SRAM).

12. A method comprising:

storing data in a local memory of an image signal processor;

generating a memory address to the local memory utilizing a memory address generator within the image signal processor; and

performing an operation on the data of the local memory located at the memory address utilizing the memory address generator to aid in image processing tasks.

13. The method of claim 12, further comprising:

storing data to be sent to the local memory in a shared memory of the image signal processor; and

storing commands in the shared memory to be performed on the data in the local memory.

14. The method of claim 13, wherein the shared memory comprises a plurality of cluster communication registers.

15. The method of claim 14, wherein the plurality of cluster communication registers include data cluster communication registers to store data and command cluster communication registers to store commands.

16. The method of claim 15, further comprising assigning a pair of cluster communication registers to one of a plurality of memory address generators, each memory address generator to generate a memory address to the local memory within

the image signal processor and to perform an operation on the data of the local memory located at the memory address to aid in image processing tasks.

17. The method of claim 16, further comprising arbitrating access to the local memory by the plurality of memory address generators.

18. The method of claim 14, wherein the plurality of cluster communication registers are at least 16-bit registers.

19. The image processor of claim 18, wherein 16-bit data paths couple the cluster communication registers to the memory address generators and the memory address generators to the local memory.

20. A machine-readable medium having stored thereon instructions, which when executed by a machine, cause the machine to perform the following operations comprising:

storing data in a local memory of an image signal processor;

generating a memory address to the local memory utilizing a memory address generator within the image signal processor; and

performing an operation on the data of the local memory located at the memory address utilizing the memory address generator to aid in image processing tasks.

21. The machine-readable medium of claim 20, further comprising:

storing data to be sent to the local memory in a shared memory of the image signal processor; and

storing commands in the shared memory to be performed on the data in the local memory.

22. The machine-readable medium of claim 21, wherein the shared memory comprises a plurality of cluster communication registers.

23. The machine-readable medium of claim 22, wherein the plurality of cluster communication registers include data cluster communication registers to store data and command cluster communication registers to store commands.

24. The machine-readable medium of claim 23, further comprising assigning a pair of cluster communication registers to one of a plurality of memory address generators, each memory address generator to generate a memory address to the local memory within the image signal processor and to perform an operation on the data of the local memory located at the memory address to aid in image processing tasks.

25. The machine-readable medium of claim 24, further comprising arbitrating access to the local memory by the plurality of memory address generators.

26. The machine-readable medium of claim 22, wherein the plurality of cluster communication registers are at least 16-bit registers.

27. The machine-readable medium of claim 26, wherein 16-bit data paths couple the cluster communication registers to the memory address generators and the memory address generators to the local memory.

28. An image processor system comprising:

a processor coupled to an image processor; and

a double data rate synchronous dynamic random access memory (DDR SDRAM) coupled to the image processor, the image processor including a plurality of image signal processors coupled to one another, each image signal processor including:

a local memory to store data, and

a memory command handler including a plurality of memory address generators, each memory address generator to generate a memory address to the local memory and to interpret a command to be performed on the data of the local memory located at the memory address to aid in image processing tasks.

29. The image processor system of claim 28, further comprising a shared memory coupled to the plurality of the memory address generators, the shared memory storing data to be sent to the local memory and commands to be performed by the memory address generators.

30. The image processor system of claim 29, wherein the shared memory comprises a plurality of cluster communication registers.

31. The image processor system of claim 30, further comprising a cluster communication register interface to couple the plurality of cluster communication registers to the plurality of memory address generators.

32. The image processor system of claim 30, wherein the plurality of cluster communication registers include data cluster communication registers to store data and command cluster communication registers to store commands.

33. The image processor system of claim 32, wherein a pair of cluster communication registers are assigned to each memory address generator.

34. The image processor system of claim 33, wherein each pair of cluster communication registers includes a data cluster communication register and a command cluster communication register.

35. The image processor system of claim 30, further comprising an arbiter to arbitrate access to the local memory by the memory address generators.

36. The image processor system of claim 35, wherein the plurality of cluster communication registers are at least 16-bit registers.

37. The image processor system of claim 36, further comprising 16-bit data paths that couple the cluster communication registers to the memory address generators, the memory address generators to the arbiter, and the arbiter to the local memory.

38. The image processor system of claim 37, wherein the local memory includes static random access memory (SRAM).